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09/388,766	09/02/1999	BOHR-WINN SHIH	303.513US1	4410

			EXAMINER
21186	7590	07/22/2004	SHARON, AYAL I

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ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 07/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
Office Action Summary	09/388,766	SHIH ET AL.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>13 May 2004</u>.

2a)☒ This action is **FINAL.**   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is

   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-35</u> is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-35</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage

      application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-35 of U.S. Application 09/388,766 was originally filed on 09/02/1999, and amended in an RCE filed on 9/22/03. Applicants' most recent amendment, filed 5/13/04, amends claims 25, 28, and 29. No claims have been added or cancelled.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office Action:

> A person shall be entitled to a patent unless-
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. The prior art cited is as follows:

4. IEEE Std 1364-1995. IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language. Copyright 1995. (Henceforth referred to as "**IEEE 1364**". Sections 1,3,6,7,9,12,14,18,19,22, pp. i-ix, and the Index of this 675 page reference have included in the file wrapper and have been provided to the

Applicants. The entire reference will be provided to the Applicants upon

request.).

5. The claims are subsequently recited for Applicant's convenience.

Applicant's attention is also directed to the pertinent sections of the prior

art.

6. **Claims 1-8, 12-30, and 33 are rejected under 35 U.S.C. 102(b) as being**

anticipated by IEEE 1364.

7. IEEE 1364 teaches the limitations of Claim 1:

1.   (Currently Amended) A method of simulating a node using a
simulation program that includes multiple, linked modules, the method
comprising:

executing a first circuit module that simulates a circuit having a
node, wherein the node represents a simulated electrical connection point
of the circuit;
(See IEEE 1364, especially: Section 12, pp.135-139; Section 3, p.13;
Section 6, pp.50-52;)

simultaneously executing at least one behavior module, which is
linked to the first circuit module, and which performs the functions of
(See IEEE 1364, especially: Section 12, pp.135-139; Section 9, pp.104-
106)

forcing an initial forced logic state on the node;
(See IEEE 1364, especially: Section 9, pp.104-106)

releasing the node from the forced logic state if a
predetermined condition is met,
which enables the simulation program to change a logic
state of the node
(See IEEE 1364, especially: Section 9, pp.104-106)

monitoring the released node after the node has been
released; and
(See IEEE 1364, especially: Section 9, pp.104-106; Section
14, pp.179-180; Section 18, pp.234, 246-247;)

providing an indication, in response to the monitoring, when
the node is in a pre-selected condition.
(See IEEE 1364, especially: Section 9.5.2, p.111; Section
14, pp.179-180; Section 18, pp.234, 246-247;)

8. IEEE 1364 teaches the limitations of Claim 2:

2.   (Currently Amended) The method of claim 1, wherein forcing the
initial forced logic state includes forcing to a logic zero, logic one or
high-impedance.
(See IEEE 1364, especially: Section 3, p.13)

9. IEEE 1364 teaches the limitations of Claim 3:

3.   (Original) The method of claim 1, wherein releasing the node
further comprises determining that the condition is met after passage of a
predetermined amount of time.
(See IEEE 1364, especially: Section 9, pp.106-107 and pp.114-119;
Section 14, pp.187-196; Section 18, pp.234, 246-247;)

10. IEEE 1364 teaches the limitations of Claim 4:

4.   (Currently Amended) The method of claim 3, wherein releasing the
node further comprises determining that the condition is met when the
node has been resolved.
(See IEEE 1364, especially: Section 3, p.17-19)

11. IEEE 1364 teaches the limitations of Claim 5:

5.   (Currently Amended) The method of claim 1, wherein providing an
indication includes indicating when the released node is in an unknown
logic state.
(See IEEE 1364, especially: Section 9.5.2, p.111; Section 14, pp.179-180;
Section 18, pp.234, 246-247; Section 3, p.13)

12. IEEE 1364 teaches the limitations of Claim 6:

6.   (Currently amended) The method of claim 1, further comprising
providing an error indication when the release node is in a pre-selected
condition.
(See IEEE 1364, especially: Section 9.5.2, p.111; Section 14, pp.179-180;
Section 18, pp.234, 246-247;)

13. IEEE 1364 teaches the limitations of Claim 7:

7.   (Original) The method of claim 3, further comprising selecting a user-defined time period for the predetermined amount of time.
(See IEEE 1364, especially: Section 9, pp.106-107 and pp.114-119; Section 14, pp.187-196; Section 18, pp.234, 246-247;)

14. IEEE 1364 teaches the limitations of Claim 8:

8.   (Currently Amended) A method of initializing and monitoring a simulated circuit node using a simulation program that includes multiple linked modules, the method comprising:

executing a first circuit module that simulates a circuit having a node, wherein the node represents a simulated electrical connection point of the circuit;
(See IEEE 1364, especially: Section 12, pp.135-139; Section 3, p.13; Section 6, pp.50-52;)

simultaneously executing at least one behavior module, which is linked to the first circuit module, and which performs the functions of
(See IEEE 1364, especially: Section 12, pp.135-139; Section 9, pp.104-106)

obtaining an initial node condition for the node, wherein the initial node condition is a logic state;
(See IEEE 1364, especially: Section 14, pp.179-180; Section 18, pp.234, 246-247;)

forcing the node to the initial node condition;
(See IEEE 1364, especially: Section 9, pp.104-106)

testing the node for a valid condition;
(See IEEE 1364, especially: Section 9, pp.106-107)

monitoring the node; and
(See IEEE 1364, especially: Section 14, pp.179-180; Section 18, pp.234, 246-247;)

providing an indication when the node is in an undesirable condition.
(See IEEE 1364, especially: Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;)

15. IEEE 1364 teaches the limitations of Claim 12:

12.   (Original) The method of claim 8, further comprising outputting the
condition of the simulated node.
(See IEEE 1364, especially: Section 9, p.110; Section 14, pp.179-183;
Section 18, pp.234, 246-247;)

16. IEEE 1364 teaches the limitations of Claim 13:

13.   (Original) The method of claim 8, further comprising obtaining a
simulation run time.
(See IEEE 1364, especially: Section 9, pp.106-107 and pp.114-119;
Section 14, pp.183-196, 202-204; Section 18, pp.234, 246-247;)

17. IEEE 1364 teaches the limitations of Claim 14:

14.   (Original) The method of claim 13, further comprising outputting a
final node condition when the simulation run time is completed.
(See IEEE 1364, especially: Section 9, pp.110-111; Section 14, pp.179-
183; Section 18, pp.234, 246-247;)

18. IEEE 1364 teaches the limitations of Claim 15:

15.   (Currently Amended) A computer-readable medium having
computer-executable instructions comprising:

       at least one selectable circuit module, which when executed
simulates a circuit having a node, wherein the node represents a
simulated electrical connection point of the circuit; and
(See IEEE 1364, especially: Section 12, pp.135-139; Section 3, p.13;
Section 6, pp.50-52;)

       at least one selectable behavior module, which is linkable to a
circuit module, and which when executed results in
(See IEEE 1364, especially: Section 12, pp.135-139; Section 9, pp.104-
106)

       forcing an initial forced logic state on the node;
       (See IEEE 1364, especially: Section 9, pp.104-106)

       releasing the node from the forced logic state if a predetermined
       condition is met, which enables a simulation program to change a
       logic state of the node and
       (See IEEE 1364, especially: Section 9, pp.104-106)

       monitoring the node after the node has been released; and

(See IEEE 1364, especially: Section 14, pp.179-180;
Section 18, pp.234, 246-247;)

providing an indication, in response to the monitoring, when the
node is in a preselected condition.
(See IEEE 1364, especially: Section 9.5.2, p.111; Section 14,
pp.179-180; Section 18, pp.234, 246-247;)

19. IEEE 1364 teaches the limitations of Claim 16:

16.   (Currently Amended) The medium of claim 15, having further
computer-executable instructions for forcing the initial forced logic state to
a logic zero, logic one or high-impedance.
(See IEEE 1364, especially: Section 3, p.13; Section 9, pp.104-106)

20. IEEE 1364 teaches the limitations of Claim 17:

17.   (Original) The medium of claim 15, having further
computer-executable instructions for determining that the condition is met
after passage of a predetermined amount of time.
(See IEEE 1364, especially: Section 9, pp.106-107 and pp.114-119;
Section 14, pp.179-190, 183-196, 202-204; Section 18, pp.234, 246-247;)

21. IEEE 1364 teaches the limitations of Claim 18:

18.   (Currently Amended) The medium of claim 15, having further
computer-executable instructions for determining that the condition is met
when the node a valid logic value.
(See IEEE 1364, especially: Section 3, p.13; Section 9, pp.106-113)

22. IEEE 1364 teaches the limitations of Claim 19:

19.   (Currently amended) The medium of claim 18, having further
computer-executable instructions for indicating when the release node is
in an unknown logic state.
(See IEEE 1364, especially: Section 3, p.13; Section 9, pp.104-106;
Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-
247;)

23. IEEE 1364 teaches the limitations of Claim 20:

20.   (Currently Amended) A simulation module of a simulation program,
the simulation module comprising:

an input means for inputting an initial node condition into a simulated
circuit node of a circuit module linked with the simulation module, wherein
the simulated circuit node represents a simulated electrical connection
point of the circuit module;
(See IEEE 1364, especially: Section 3, p.13; Section 6, pp.50-52; Section
9, pp.104-106; Section 12, pp.135-139;)

a conveying means for conveying the initial node condition to the
simulated circuit node;
(See IEEE 1364, especially: Section 9, pp.104-106;)

release means for releasing the simulated circuit node from the initial node
condition upon satisfaction of a condition, wherein releasing the simulated
circuit node enables the simulation program to change a logic state of the
simulated circuit node;
(See IEEE 1364, especially: Section 9, pp.104-106;)

a monitoring means for monitoring the simulated circuit node for a node
condition; and
(See IEEE 1364, especially: Section 9.5.2, p.111; Section 14, pp.179-180;
Section 18, pp.234, 246-247;)

an output means, responsive to the monitoring means, for outputting an
indication when the node condition is in an undesirable state.
(See IEEE 1364, especially: Section 9, pp.110-111; Section 14, pp.179-
183; Section 18, pp.234, 246-247;)

24. IEEE 1364 teaches the limitations of Claim 21:

21.   (Original) The module of claim 20, further comprising an output
means for outputting the node condition.
(See IEEE 1364, especially: Section 9, pp.110-111; Section 14, pp.179-
183; Section 18, pp.234, 246-247;)

25. IEEE 1364 teaches the limitations of Claim 22:

22.   (Original) The module of claim 20, further comprising an input
means for inputting a simulation run time.
(See IEEE 1364, especially: Sections 9.2, 9.3, pp.103, and 106-107 and
pp.114-119; Section 14, pp.179-190, 183-196, 202-204; Section 18,
pp.234, 246-247;)

26. IEEE 1364 teaches the limitations of Claim 23:

23.   (Original) The module of claim 22, further comprising an output
means for outputting a final node condition at completion of the simulation
run time.
(See IEEE 1364, especially: Section 9, pp.110-111; Section 14, pp.179-
183; Section 18, pp.234, 246-247;)

27.IEEE 1364 teaches the limitations of Claim 24:

24.   (Currently Amended) A computerized system for initializing and
monitoring a simulated circuit node, the system comprising:

     a circuit simulation tool;
     (See IEEE 1364, especially: Section 1.2)

     at least one selectable circuit module, which when executed
simulates a circuit having the simulated circuit node, wherein the
simulated circuit node represents a simulated electrical
connection point of the circuit; and
     (See IEEE 1364, especially: Section 12, pp.135-139)

     at least one selectable behavior module, which is linkable to a
circuit module, and which includes
     (See IEEE 1364, especially: Section 9, pp.98-99)

     a first input means for inputting an initial node condition;
     (See IEEE 1364, especially: Section 9, pp.104-106)

     a conveying means for conveying the initial node condition to the
simulated circuit node;
     (See IEEE 1364, especially: Section 9, pp.104-106)

     a release means for releasing the initial node condition, wherein
releasing the initial node condition enables the circuit simulation tool to
change a logic state of the simulated circuit node;
     (See IEEE 1364, especially: Section 9, pp.104-106)

     a monitoring means for monitoring the simulated circuit node for a
node condition;
     (See IEEE 1364, especially: Section 14, pp.179-180;
     Section 18, pp.234, 246-247;)

     a first output means for outputting an indication when the node
condition is in an undesirable state;
     (See IEEE 1364, especially: Section 9, pp.110-111;
     Section 14, pp.179-183; Section 18, pp.234, 246-247;)

a second input means for inputting a simulation run time; and
(See IEEE 1364, especially: Sections 9.2, 9.3, pp.103, and 106-107
and pp.114-119; Section 14, pp.179-190, 183-196, 202-204;
Section 18, pp.234, 246-247;)

a second output means for outputting a final node condition at
completion of the simulation run time.
(See IEEE 1364, especially: Section 9, pp.110-111;
Section 14, pp.179-183; Section 18, pp.234, 246-247;)

28. IEEE 1364 teaches the limitations of Claim 25:

25. (Currently Amended) An HDL initial condition module comprising:

a means for forcing a logic level on a simulated circuit node;
(See IEEE 1364, especially: Section 9, pp.104-106)

a means for maintaining the logic level of the simulated circuit node
until a release condition is met, wherein
(See IEEE 1364, especially: Section 9, pp.104-106)

the simulated circuit node represents a simulated electrical
connection point of a simulated circuit and the simulated circuit is
produced by an HDL circuit module that is linkable to the HDL initial
condition module, and
(See IEEE 1364, especially: Section 3, pp.13-16; Section 12, pp.135-139;)

a simulation program is able to change a logic state of the
simulated circuit node after the release condition is met.
(See IEEE 1364, especially: Section 9, pp.104-106)

a means for monitoring the simulated circuit node after the
simulated circuit node has been released; and
(See IEEE 1364, especially: Section 9, pp.104-106; Section 14, pp.179-
180; Section 18, pp.234, 246-247;)

a means for providing an indication, in response to the monitoring,
when the simulated circuit node is in a preselected condition.
(See IEEE 1364, especially: Section 9.5.2, p.111; Section 14, pp.179-180;
Section 18, pp.234, 246-247;)

29. IEEE 1364 teaches the limitations of Claim 26:

26.   (Currently Amended) The module of claim 25 wherein the release condition is when a known logic state can be determined for the simulated circuit node.
(See IEEE 1364, especially: Section 9, pp.104-106, 110-111;
            Section 14, pp.179-183; Section 18, pp.234, 246-247;)

30. IEEE 1364 teaches the limitations of Claim 27:

27.   (Original) The module of claim 25 wherein the logic level is a value defined by an HDL executable simulation program.
(See IEEE 1364, especially: Section 9, pp.104-106)

31. IEEE 1364 teaches the limitations of Claim 28:

28.   (Currently Amended) <u>The module of claim 25, further comprising:</u>

an initial condition release means, which enables <u>the</u> simulation program to change <u>the</u> logic level after the release condition is met; and
(See IEEE 1364, especially: Section 3, pp.13-16; Section 9, pp.104-106, 110-111; Section 12, pp.135-139; Section 14, pp.179-183; Section 18, pp.234, 246-247;)

a simulated circuit node error detection means, which monitors the simulated circuit node for a node condition.
(See IEEE 1364, especially: Section 9, pp.104-106, 110-111;
Section 14, pp.179-183; Section 18, pp.234, 246-247;)

32. IEEE 1364 teaches the limitations of Claim 29:

29.   (Currently Amended) <u>The module of claim 25, wherein the</u>

means for maintaining <u>the</u> logic level of <u>the</u> simulated circuit node <u>maintains the logic level </u>for a predetermined period
of time, and
(See IEEE 1364, especially: Section 3, pp.13-16; Sections 9.2, 9.3, pp.103-107, 110-111, 114-119; Section 12, pp.135-139; Section 14, pp.179-196, 202-204; Section 18, pp.234, 246-247;)

<u>wherein the module further comprises;</u>

means for releasing an initial condition after <u>the</u> release condition is met, wherein the predetermined period of time is a simulation run time defined by an HDL simulation executable program.

(See IEEE 1364, especially: Sections 9.2, 9.3, pp.99-104, and 106-107
and pp.114-119; Section 14, pp.179-190, 183-196, 202-204; Section 18,
pp.234, 246-247;)

33. IEEE 1364 teaches the limitations of Claim 30:

30.   (Original) The module of claim 29, wherein the predetermined
period of time is a user-defined period of time.
(See IEEE 1364, especially: Section 9, pp.99-104, 106-107 and pp.114-
119; Section 14.3, 14.5, 14.8; Section 18, pp.234, 246-247;)

34. In regards to Claim 33, IEEE 1364 teaches a simulated HDL circuit device

(Section 1, pp. iii-iv, 1-4), a plurality of HDL modules (Section 12, pp.135-

139), nodes (Section 6, pp.50-52), behavior modules (Section 9),

assigning/de-assigning and forcing/releasing node values, and condition

statements (Section 9, pp.104-106), monitoring node values (Section

9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;), and

outputting node values (Section 9, pp.110-111; Section 14, pp.179-183;

Section 18, pp.234, 246-247;), and outputting an undesirable state

(Section 9, p.111).

Claim Rejections - 35 USC § 103

35. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for

all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically
disclosed or described as set forth in section 102 of this title, if the
differences between the subject matter sought to be patented and the
prior art are such that the subject matter as a whole would have been
obvious at the time the invention was made to a person having ordinary
skill in the art to which said subject matter pertains. Patentability shall not
be negatived by the manner in which the invention was made.

36. The prior art cited is as follows:

37. IEEE Std 1364-1995. IEEE Standard Hardware Description Language

    Based on the Verilog® Hardware Description Language. Copyright 1995.

    (Henceforth referred to as **"IEEE 1364"**. Sections

    1,3,6,7,9,12,14,18,19,22, pp. i-ix, and the Index of this 675 page reference

    have included in the file wrapper and have been provided to the

    Applicants. The entire reference will be provided to the Applicants upon

    request.).

38. The claims are subsequently recited for Applicant's convenience.

    Applicant's attention is also directed to the pertinent sections of the prior

    art.

39. **Claims 9-11, 31-32, and 34-35 are rejected under 35 U.S.C. 103(a) as**

    being unpatentable over IEEE in view of Official Notice.

40. In regards to Claim 9, IEEE 1364 teaches the functionalities of the

    unknown state (Section 3, p.1), monitoring the state (Section 9.5.2, p.111;

    Section 14, pp.179-180; Section 18, pp.234, 246-247;), looping

    statements with conditions (Section 9, pp.111-114), and forcing nodes

    (Section 9, pp.104-106).

    However, IEEE 1364 does not expressly teach the limitations of

    Claim 9:

    9.   (Currently Amended) The method of claim 8, wherein the initial
    node condition is forced again if the testing indicates that the node has an
    unknown logic value.

Combining the features taught by IEEE 1364 in the configuration claimed

by the Applicants is a matter of design choice.

Official Notice is given that it would have been obvious to one of

ordinary skill in the art at the time the invention was made to modify the

features detailed above to as to enable re-forcing a node's value if testing

indicates that a node's value is unknown, because it is impossible to do

analysis on a node with an unknown value.

41. In regards to Claim 10, IEEE 1364 teaches the functionalities of the

unknown and valid logic states (Section 3, p.1), monitoring the state

(Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-

247;), looping statements with conditions (Section 9, pp.111-114), and

forcing nodes (Section 9, pp.104-106).

However, IEEE 1364 does not expressly teach the limitations of

Claim 10:

10.   (Currently Amended) The method of claim 9, wherein the initial
node condition is forced and simulation is repeated until the node has a
valid logic value.

Combining the features taught by IEEE 1364 in the configuration claimed

by the Applicants is a matter of design choice.

Official Notice is given that it would have been obvious to one of

ordinary skill in the art at the time the invention was made to modify the

features detailed above to as to enable re-forcing a node's value if testing

indicates that a node's value is unknown, because it is impossible to do

analysis on a node with an unknown value. Moreover, it is preferable to do

analysis on a node that has a derived value as opposed to one with an

arbitrarily assigned value.

42. In regards to Claim 11, IEEE 1364 teaches the functionalities of the

unknown and valid logic states (Section 3, p.1), monitoring the state

(Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-

247;), looping statements with conditions (Section 9, pp.111-114), and

forcing nodes (Section 9, pp.104-106).

However, IEEE 1364 does not expressly teach the limitations of

Claim 11:

11.   (Currently Amended) The method of claim 10, wherein monitoring
only occurs after the node has a valid logic value.

Combining the features taught by IEEE 1364 in the configuration claimed

by the Applicants is a matter of design choice.

Official Notice is given that it would have been obvious to one of

ordinary skill in the art at the time the invention was made to modify the

features detailed above to as to enable re-forcing a node's value if testing

indicates that a node's value is unknown, because it is impossible to do

analysis on a node with an unknown value. Moreover, it is preferable to do

analysis on a node that has a derived value as opposed to one with an

arbitrarily assigned value.

43. In regards to Claim 31, IEEE 1364 teaches a simulated HDL circuit device

(Section 1, pp. iii-iv, 1-4), HDL modules (Section 12, pp.135-139), nodes

(Section 6, pp.50-52), assigning/forcing node values, and condition statements (Section 9, pp.104-106), monitoring node values (Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;), and outputting node values (Section 9, pp.110-111; Section 14, pp.179-183; Section 18, pp.234, 246-247;), and outputting an undesirable state (Section 9, p.111).

IEEE 1364, however, does not expressly teach the use of exactly two modules. (Section 12 enables the implementation of an undefined number of modules). Moreover, IEEE 1364 does not expressly teach that the commands for assigning, monitoring, or outputting node values are implemented as "sub-modules". Finally, IEEE 1364 does not expressly teach the following limitation:

> a second output submodule outputting a second indication when the second node condition is in an undesirable state; and wherein the first conveyance submodule additionally conveys the first initial node condition to the second input submodule.

In regards to the use of exactly two modules, Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to create two modules, because some simple circuits have only two components of interest.

In regards to referring to commands for assigning, monitoring, or outputting node values are implemented as "sub-modules", Examiner interprets Applicant's use of the term "sub-module" as being functionally

equivalent to what is commonly known in the art under the following names: command, function, sub-routine.

Finally, in regards to the first module conveying the initial code condition to the second module (which had an undesirable state), Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a circuit with a known state pass on its state to a linked circuit with an unknown state, because this represents the propagation of a signal in a circuit.

44. In regards to Claim 32, IEEE 1364 teaches a simulated HDL circuit device (Section 1, pp. iii-iv, 1-4), HDL modules (Section 12, pp.135-139), nodes (Section 6, pp.50-52), assigning/de-assigning and forcing/releasing node values, and condition statements (Section 9, pp.104-106), monitoring node values (Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;), and outputting node values (Section 9, pp.110-111; Section 14, pp.179-183; Section 18, pp.234, 246-247;), and outputting an undesirable state (Section 9, p.111).

IEEE 1364, however, does not expressly teach the use of exactly three modules. (Section 12 enables the implementation of an undefined number of modules). In addition, IEEE 1364 does not expressly teach the following limitation:

a third HDL module, linked to the circuit HDL module, the third HDL module including

a release condition means for releasing the second simulated node on a release condition, wherein releasing the second simulated node

enables a simulation program to change a logic level of the second simulated node.

wherein the first node condition output means outputs the first node condition to the second input means if the release condition is valid.

In regards to the use of exactly three modules, Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to create two modules, because some simple circuits have only three components of interest.

In addition, in regards to the first module conveying the initial code condition to the second module (which had a released, and therefore changeable, state), Official Notice is given that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a circuit with a known state pass on its state to a linked circuit with an unknown state, because this represents the propagation of a signal in a circuit.

45. In regards to Claim 34, IEEE 1364 teaches the functionalities of a simulated HDL circuit device (Section 1, pp. iii-iv, 1-4), HDL modules (Section 12, pp.135-139), nodes (Section 6, pp.50-52), unknown and valid logic states (Section 3, p.1), assigning/de-assigning and forcing/releasing node values (Section 9, pp.104-106), monitoring node values (Section 9.5.2, p.111; Section 14, pp.179-180; Section 18, pp.234, 246-247;), and outputting node values (Section 9, pp.110-111; Section 14, pp.179-183; Section 18, pp.234, 246-247;), outputting an undesirable state (Section 9,

p.111), condition statements (Section 9, pp.106-107), and looping

statements with conditions (Section 9, pp.111-114)

However, IEEE 1364 does not expressly teach that a simulation is

repeated ("continuing in phase one") until the node has a valid logic value.

Official Notice is given that it would have been obvious to one of

ordinary skill in the art at the time the invention was made to modify the

features detailed above to as to enable repeatedly re-forcing and then re-

releasing a node's value if testing indicates that a node's value is

unknown, because it is impossible to do analysis on a node with an

unknown value. Moreover, it is preferable to do analysis on a node that

has a derived value as opposed to one with an arbitrarily assigned value.

In addition, it sometimes takes time for a circuit to get defined inputs from

its input circuits.

46. IEEE 1364 teaches the limitations of Claim 35:

> 35.   (Original)   The method of claim 34, wherein simulation
> completion is a user defined time period.
> (See IEEE 1364, especially: Sections 9.2, 9.3, pp.103, and 106-107
> and pp.114-119; Section 14, pp.179-190, 183-196, 202-204; Section 18,
> pp.234, 246-247;)

Response to Amendment filed 5/13/2004

Re: Claim Rejections - 35 USC § 102

47. In regards to the claims rejected under 35 USC §102, (Claims 1-8, 12-30,

and 33), Applicants argue (p.12) that

> Further, although IEEE 1364 describes various capabilities of Verilog HDL, these

capabilities are described in conjunction with a simulation program module, and not in conjunction with a behavior module that includes the limitations of Applicant's claims.

Examine respectfully refers the Applicants to IEEE 1364, which enables Behavioral Modeling (see IEEE 1364, Section 9 "Behavioral Modeling", pp.98-124) in addition to Gate and Switch Level Modeling (see IEEE 1364, Section 7 "Gate and Switch Level Modeling"). The IEEE 1364 reference specifically teaches (p.98) that:

> The language constructs introduced so far [Gate and Switch Level Modeling] allow hardware to be described at a relatively detailed level. ... however, these constructs do not provide the power of abstraction necessary for describing complex high level aspects of a system. The procedural constructs described in this section are well suited to tackling problems such as describing a microprocessor or implementing complex timing checks.

Examiner therefore respectfully disagrees with Applicants' argument that "these capabilities are described ... not in conjunction with a behavior module that includes the limitations of Applicant's claims."

48. Applicants also argue in the amendment (pp.11-12) that IEEE 1364 does not teach the following limitations:

> - simultaneously executing at least one behavior module, which is linked to the first circuit module . . . (claims 1-7, 8, 12-14)

In IEEE 1364, Section 11 "Tasks and Functions" teaches (p.125) that:

> Tasks and functions provide the ability to execute common procedures from several different places in a description. They also provide a means of breaking up large procedures into smaller ones to make it easier to read and debug the source descriptions. This section describes the differences between tasks and functions, describes how to define and invoke tasks and functions, and presents examples of each.

Moreover, in regards to tasks, Section 11 teaches (p.126) that:

> The task declaration shall not declare a net data type. The body of the task shall contain zero or more behavioral statements (See Section 9).

Moreover, in regards to modules, Section 12 teaches (p.126) that:

The syntax and semantics of arrays of instances defined for gates and primitives
apply for modules as well.

The "Syntax for Module" in Fig.12-1 (p.136) also shows that "gate

instantiation" is one of the elements of Module definition,

In addition, in regards to the relationship between tasks and

modules, Section 12.5 teaches (p.126) that tasks can be embedded within

modules (See Fig. 12-3, and accompanying text on pp.150-151).

Therefore, examiner respectfully disagrees with the Applicants'

argument that IEEE 1364 does not teach the limitation "simultaneously

executing at least one behavior module, which is linked to the first circuit

module".

49. Applicants also argue in the amendment (pp.11-12) that IEEE 1364 does

not teach the following limitations:

- at least one behavior module, which when executed results in
    forcing an initial forced logic state (or initial node condition) on the node
        of at least one selectable circuit module,
    releasing the node from the forced logic state if a predetermined
        condition is met,
    monitoring the node after the node, and
    providing an indication, in response to the monitoring, when the node is
        in a pre-selected condition (or an undesirable state).
(claims 1-7, 8, 12-14, 15-19, 20-23, 33)

Examiner respectfully disagrees. Section 9, pp.104-106 of IEEE 1364

teaches the forcing and releasing of nodes. Section 9, p.106, teaches the

use of the conditional statement. Section 14, pp.179-180, teaches strobed

and continuous monitoring.

Moreover, the following sections all describe methods of providing

indications when a node is in a pre-selected condition (or undesirable

state): Section 9.5.2, p.111, which teaches "constant expression in a case

statement", where the "constant expression" is compared against case

item expressions, and Section 14, pp.179-180, teaches strobed and

continuous monitoring, which "provides the ability to monitor and display

the values of any variables or expressions specified as arguments to the

task."

Therefore, examiner respectfully disagrees with the Applicants'

argument that IEEE 1364 does not teach the claimed limitations.

50. Applicants also argue in the amendment (pp.11-12) that IEEE 1364 does

not teach the following limitations:

> - an HDL module comprising
> a means for forcing a logic level on a simulated circuit node;
> a means for maintaining the logic level of the simulated circuit node until a
>   release condition is met, wherein . . . a simulation program is able to
>   change a logic state of
> the simulated circuit node after the release condition is met;
> a means for monitoring the simulated circuit node after the simulated circuit node
>   has been released; and
> a means for providing an indication, in response to the monitoring, when the
>   simulated circuit node is in a pre-selected condition.
> (claims 25-27, 28-30)

Examiner respectfully disagrees, for the reasons stated in the immediately

preceding paragraph.

Re: Claim Rejections - 35 USC § 103

51. In regards to the claims rejected under 35 USC §103, (Claims 9-11, 31-32

and 34-35), which were rejected under IEEE 1364 in view of official notice,

Applicants request (p.13) that the Examiner provide a reference that

describes the elements used in the Official Notice.

52. In regards to claims 9, 10, 11, and 34, Examiner took Official Notice as

follows:

"Official Notice is given that it would have been obvious to one of ordinary skill in the
art at the time the invention was made to modify the features detailed above as to enable
re-forcing a node's value if testing indicates that a node's value is unknown, because it is
impossible to do analysis on a node with an unknown value." (See p. 12, section 40)

In light of Applicants' request (pp.13-15 of the amendment), Examiner is

providing a copy of the IEEE Standard 1164-1993: Multivalue Logic

System for VHDL Model Interoperability. Examiner notes that the VHDL

language is a direct competitor to the Verilog language, and provides

almost the same functionality as the Verilog language.

In regards to the specific Official Notice rejection, pp.4-5 of the

IEEE Std. 1164-1993 contain truth tables of nine different signals (U, X, 0,

1, Z, W, L, H, and '-'), where 'X' represents a "forcing unknown", while a

'W' represents a "weak unknown". The truth tables on pp.4-5 show that

these signals remain "unknown" unless they go through an "AND" gate

together with an '0' signal, or go through an "OR" gate with a '1' signal. In

other words, the signals remain unknown unless they are forced to either

'0' or '1'.

On the other hand, a '1' signal input into an "AND" gate or a '0'

signal input into an "OR" gate produces an output which provides

information about the other signal being input into the gate. This evidence

supports Examiner's Official Notice in the previous Office Action.

53. In regards to claims 10, 11, and 34, Examiner took Official Notice as

follows:

. . . it is preferable to do analysis on a node that has a derived value as opposed to one with an arbitrarily assigned value." (claims 10, 11, 34)

The same evidence from IEEE Std. 1164-1993, described in the immediately preceding paragraph, applies to this argument as well.

54. In regards to claims 31, and 32, Examiner took Official Notice as follows:

. . it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a circuit with a known state pass on its state to a linked circuit with an unknown state, because this represents the propagation of a signal in a circuit." (claims 31, 32)

The same evidence from IEEE Std. 1164-1993, described in the The same evidence from IEEE Std. 1164-1993, described in the immediately preceding paragraph, applies to this argument as well.

55. In regards to claims 31, and 32, Examiner took Official Notice as follows:

. . it would have been obvious to one of ordinary skill in the art at the time the invention was made to create two modules, because some simple circuits have only two components of interest." (claim 31)

. . it would have been obvious to one of ordinary skill in the art at the time the invention was made to create two modules, because some simple circuits have only three components of interest." (claim 32)

In IEEE 1364, the primary reference used in the rejections recited in the previous Office Action, Section 11 "Tasks and Functions" teaches (p.125) that:

> Tasks and functions provide the ability to execute common procedures from several different places in a description. They also provide a means of breaking up large procedures into smaller ones to make it easier to read and debug the source descriptions. This section describes the differences between tasks and functions, describes how to define and invoke tasks and functions, and presents examples of each.

Examiner finds that the Applicants' limitations that claim exactly two modules is a matter of design choice. In re Kuhle, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) and MPEP §2144.04.

56. In regards to claim 34, Examiner took Official Notice as follows:

> . . In addition, it sometimes takes time for a circuit to get defined inputs from its input circuits." (claim 34)

Raimi et al., U.S. Patent 5,680,332, teaches the measurement of the test coverage of digital simulation of a circuit (see Abstract). It generates output that shows which sets of circuit states were and were not visited and which transitions allowed by the State Bin Transition Relation were and were not taken during the simulation. (see Abstract)

This is analogous to the claimed invention, which test circuits by using a module that controls initial circuit test conditions and provides error detection for simulated circuit nodes (see specification, pp.2-3).

Raimi expressly teaches (col.2, lines 25-27) that "The Composite Circuit Model" is translated into implicit FSM representations utilizing BDDs. A State Bin Transition Relation is formed which represents allowable transitions among user-specified sets of states or State Bins, and a representation of the reachable State Bins is built."

An FSM is a Finite State Machine, and FSMs inherently require several clock cycles to propagate state changes though the various states. A circuit modeled in such a way would inherently have delays in propagating new input states throughout the circuit -the propagation would not be instantaneous. This evidence supports Examiner's Official Notice in the previous Office Action.

Conclusion

57. Applicant's arguments filed 5/13/2004 have been fully considered but they are not persuasive.

58. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Applicant should submit an argument under the heading "Remarks" pointing out disagreements with the examiner's contentions. Applicant must also discuss the references applied against the claims, explaining how the claims avoid the references or distinguish from them.

Correspondence Information

Any inquiry concerning this communication or earlier

communications from the examiner should be directed to Ayal I. Sharon

whose telephone number is

(703) 306-0297. The examiner can normally be reached on Monday

through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful,

the examiner's supervisor, Kevin Teska can be reached on (703) 305-

9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

Fax: (703) 872-9306

Any inquiry of a general nature or relating to the status of this

application or proceeding should be directed to the receptionist, whose
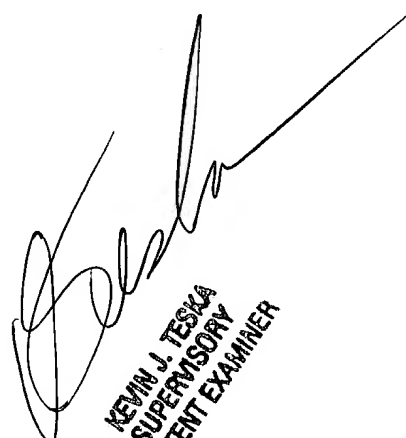
telephone number is:

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Art Unit 2123

July 15, 2004

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